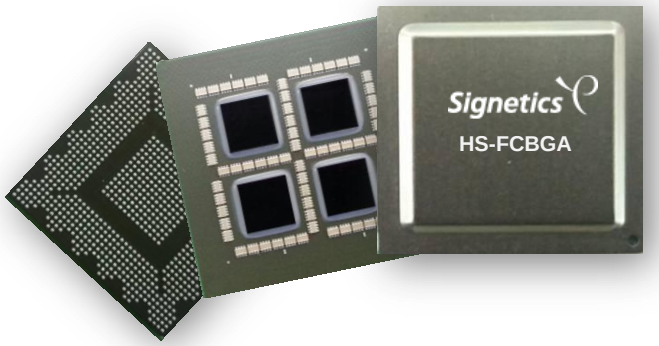
fc-BGA
Die exposed / MCM / HS / SiP



Description

Between the die and substrates, Flip Chip interconnection has been replace conventional wire bonding. Flip Chip interconnections provide high electrical performance demand in ASICs, Memory applications where high frequency, high speed are required.

Using Flip Chip interconnect improves package electrical performance by shorter electrical path, removing high inductance wires and fc-BGA is available in a high thermal performance with heat spreader. The array of bumps under the chip also allows to reduce the die with the wafer cost.

Signetics offers flip chip packages both BGA and CSP type and continues to develop the various range of flip chip packages to meet customers' request.

Package Sizes	7x7mm ~ 45x45mm
I/O Counts	100 ~ 1936

Features

- 4-10 layer, build-up substrates w/ strip & unit base
- 65N/LK, 40N/ELK, 28N/ELK
- Eutectic, Hi-Pb, Pb-free & Cu pillar bumps
- Nitride, Polyimide, BCB wafer passivation
- Ni-Au, Ni-Pd-Au, SOP (solder on pad), OSP (organic solder preservative), Immersion Tin finish
- Available in thermally enhanced version with heat spreader (HS-FCBGA)
- Also available with multiple components & chip to form a system-in-package version (FCBGA-SIP)
- Packing : JEDEC tray
- Package configuration : JEDEC standards

Applications

- High speed/ bandwidth Ethernet or network processes.
- HDD Storages
- Graphics Processing Units

www.signetics.com

Signetics (HQ)
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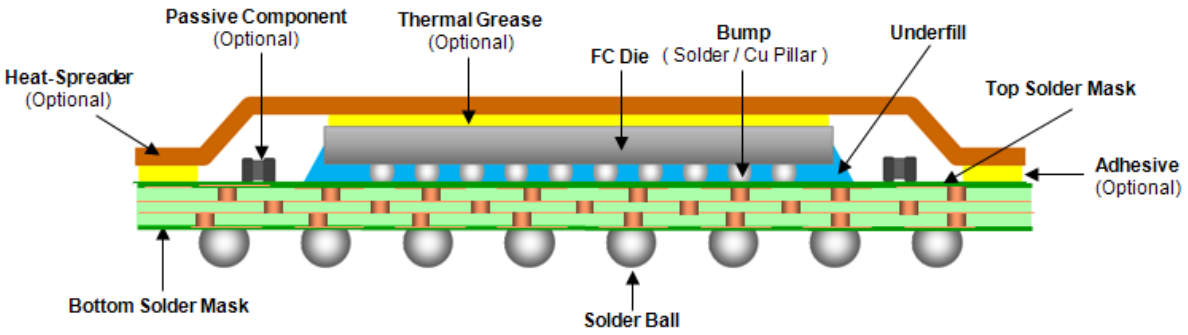
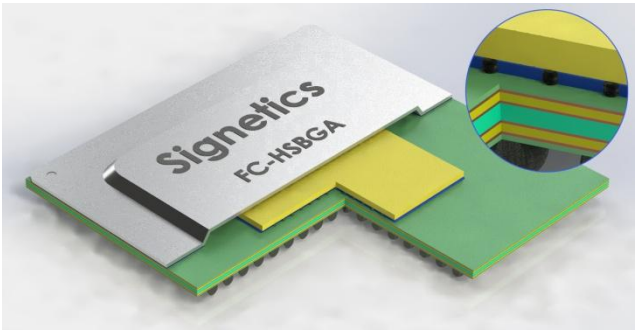
fc-BGA
Die exposed / MCM / HS / SiP

Signetics



Reliability

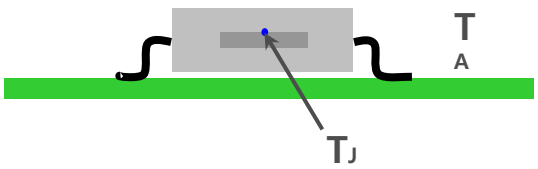
MSL Level	JEDEC Level 3
Temp Cycling	-55°C/125°C, 1000 cycles
Unbiased HAST	130°C/85% RH, 2 atm, 96hrs
High Temp Storage	150°C, 1000hrs



Thermal Data

BODY SIZE	Ball Count	Theta JA (°c/w)
FCHSBGA19X19	784B	14.54
FCHSBGA 23X23	625B	12.96

• JEDEC STD 2S2P PCB, Still air

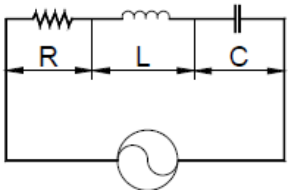


Electrical Data

- 15X15mm Body, 323B
- Simulation Frequency : 5.8GHz

Resistance (mΩ)	1520~4840
Inductance (nH)	3.52~11.85
Capacitance (pF)	0.57~1.38

• Results dependent on body size, die size, and Substrate design etc..



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