

## Description

fc-QFN (Flip-Chip Quad Flat No lead) is a low cost molded package using flip chip interconnections on a copper lead frame substrate.

This package provides small form factor compared with conventional QFP packages. And it also provides better electrical performance due to the short electrical path.

fc-QFN Packages include an exposed Thermal pad to improve heat transfer out of the IC. Exposed thermal pad can give a low inductance ground connection.

<b>Package Sizes</b>	3x3mm ~ 12x12 mm
<b>I/O Counts</b>	8 ~ 164

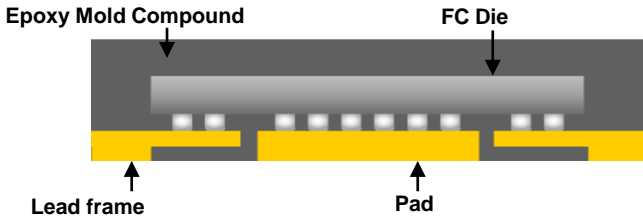
## Features

- Cu pillar with Sn/Ag plated
- Excellent electrical and thermal performance
- Minimum lead pitch 0.4mm
- Up to 12 x 12mm body size available
- Multiple lead rows available
- Body thickness of 1.0mm and below
- Low cost lead frame packaging solution
- Electrical performance achieved by shorter lead lengths
- Cost efficient vs. substrate packages
- Thermal performance enhanced by having the die pad soldered to the PCB
- VQFN Option Thickness:  $0.85 \pm 0.05\text{mm}$
- WQFN Option Thickness :  $0.75 \pm 0.05\text{mm}$
- UQFN Option Thickness :  $0.65 \pm 0.05\text{mm}$
- JECEC Level 1 compliant (defending on body size)

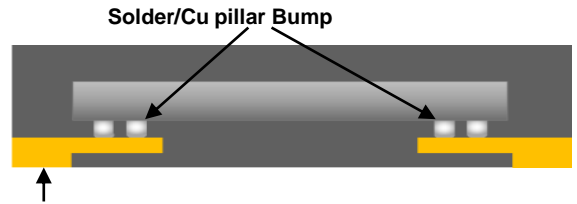
## Applications

- Applications include cellular phones
- DSPs, USB Controllers
- HD devices, Micro-Controllers
- Wireless LAN

## Exposed pad

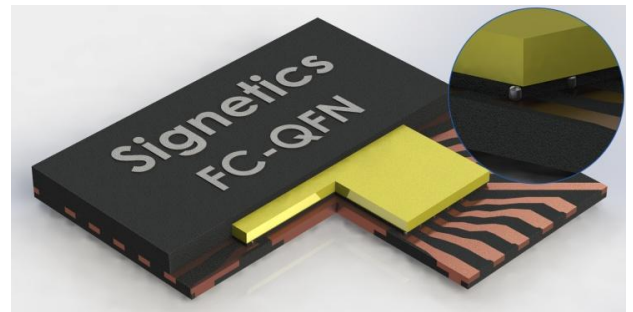


## Non-exposed pad



## Reliability

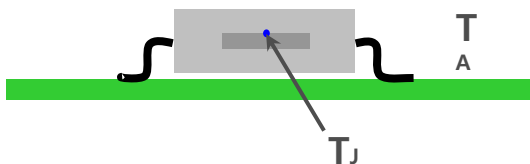
<b>MSL Level</b>	JEDEC Level 3
<b>Temp Cycling</b>	-65°C/150°C, 1000 cycles
<b>Autoclave</b>	130°C/85% RH, 2 atm, 96hrs
<b>High Temp Storage</b>	150°C, 1000hrs



## Thermal Data

BODY SIZE	Ball Count	Theta JA (°c/w)
4X4mm	24	29.23
6X6mm	44	22.44

- JEDEC STD 2S2P PCB, Still air



## Electrical Data

- 5X5mm Body, 36LD
- Simulation Frequency : 800MHz

<b>Resistance (mΩ)</b>	28~42
<b>Inductance (nH)</b>	0.40~0.65
<b>Capacitance (pF)</b>	0.09~0.12

- Results dependent on body size, die size, and Substrate design etc..

